PART 3 BCD OUTPUT MODULE FOR 7054/7144

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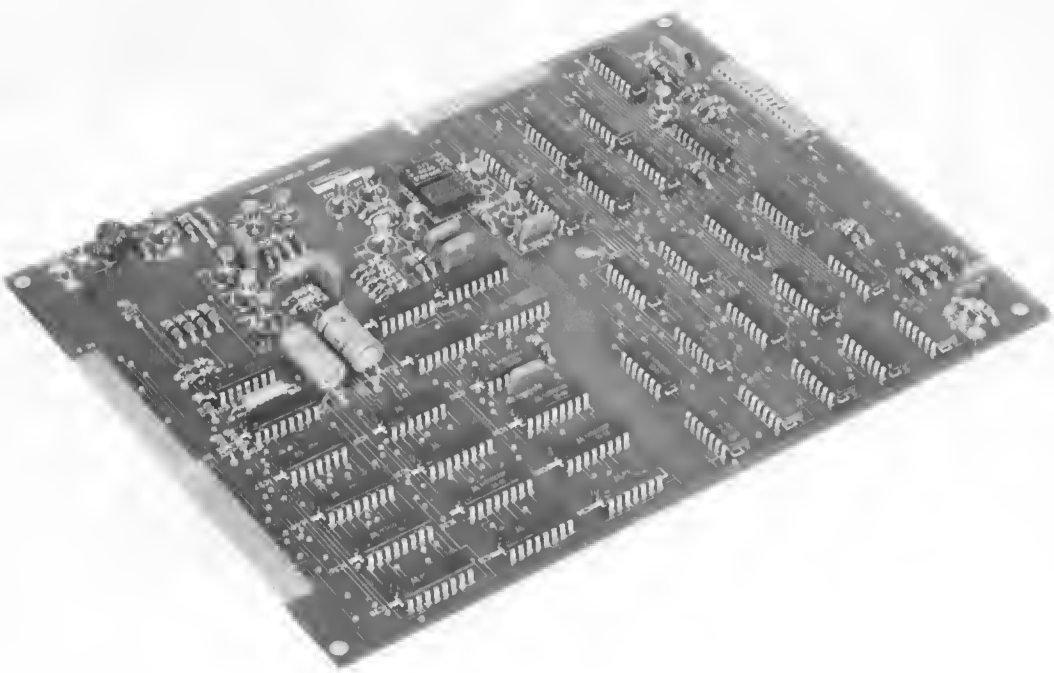

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THE SOLARTRON ELECTRONIC GROUP LIMITED
FARNBOROUGH HAMPSHIRE ENGLAND GU14 7PW
TEL: FARNBOROUGH 44433 (STD 0252)
CABLES: SOLARTRON FARNBOROUGH HANTS
TELEX: 858245 SOLARTRON FARNBOROUGH

TECHNICAL MANUAL

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CONTENTS

SECTION 1 General

INTRODUCTION

The 7054/7144 BCD Output Module is used on the 7054 and 7144 DMM, the difference in their scale lengths being catered for by a set of links on the Module pcb. A common pcb is used for both types of instrument, Solartron Part Number 70509004.

The BCD Output Module provides an isolated parallel BCD output from the 7054/7144 DMM, consisting of the magnitude, and the range (in BCD code). The DMM mode is manually selected and is therefore not programmable.

The BCD Output Module operates in the normal sample/print command closed loop mode, generally associated with a system incorporating a Recorder (Teleprinter, Typewriter, etc.) and its Drive Unit, or similar devices which provide the necessary TTL compatible input/output. The following equipment is recommended for use with the 7054/7144 DMM.

SOLARTRON A290 RECORDER DRIVE UNIT

Provides a simple recording system, the RDU controlling the DMM and driving the desired recording device.

SOLARTRON A226 PROGRAMMER

Provides the facilities of a 10 channel scanning system with high and low limit detection. Can also be supplemented by the A290 RDU.

The Module provides complete isolation between the DMM and the peripheral, and removal of the BCD Output Module from the DMM has no significant affect on the latter's performance.

Fig. 1.1 shows the physical location of the BCD Output Module on the 7144 DMM.

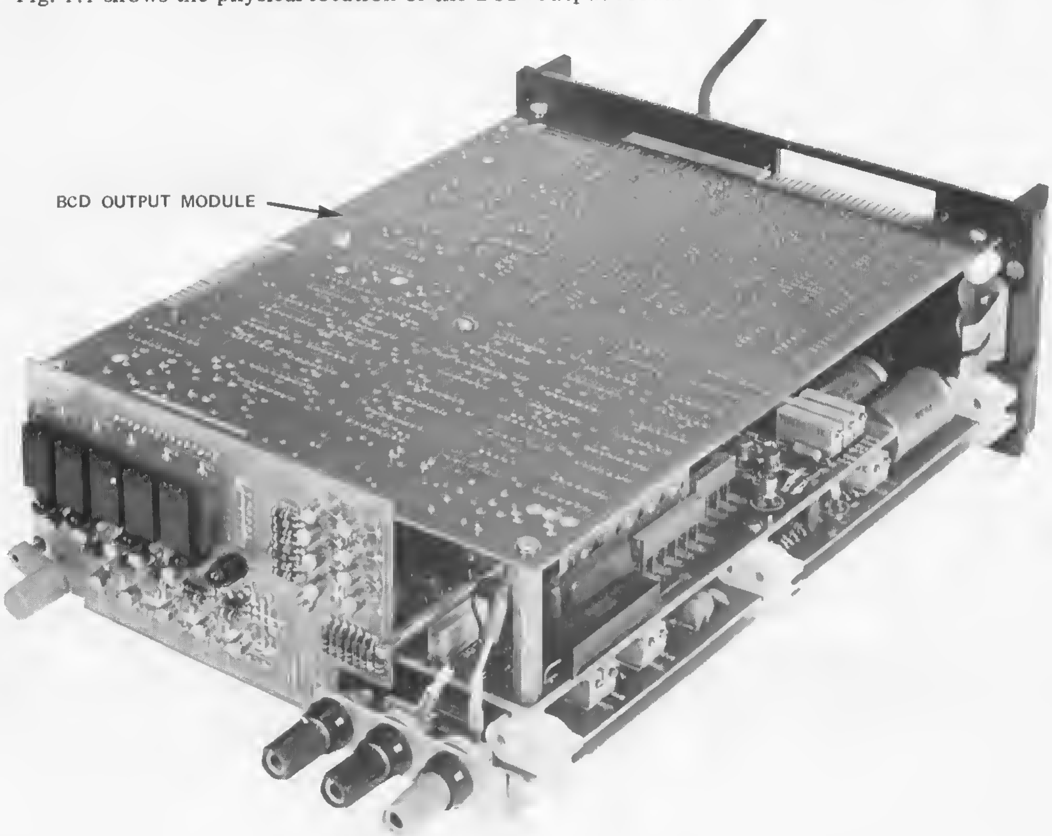


Fig. 1.1 View of the 7144 DMM with case removed.

SECTION 2 Operation

This section provides all the necessary instructions concerning preliminary checks and operating procedures required when the BCD Output Module is to be used.

PRELIMINARY CHECKS

Before using the instrument the following checks are necessary:-

CAUTION:- IT IS ESSENTIAL THAT THE INSTRUMENT BE ISOLATED FROM THE MAINS SUPPLY BEFORE OUTER CASE REMOVAL, DUE TO UNCOVERED TERMINALS ON THE ON/OFF SWITCH.

BEWARE OF GUARD POTENTIAL ON GUARD PLATE WITH INSTRUMENT CASE REMOVED.

(a) Remove the DMM case and check that the BCD Output Module is correctly linked for the type of DMM used. Fig. 2.1 shows the location of the links and the floating section power connections.

LINK 1 :- For 7054

LINK 2 :- For 7144

(b) Check for correct earth connections.

NOTE:- The 0V(E) for the BCD output is normally connected internally by a wire to the 7054/7144 mains earth. If a mains earth is not used on the 7054/7144, or if the wire has been removed, the 0V(E) connection may be made at the peripheral end to avoid an earth loop.

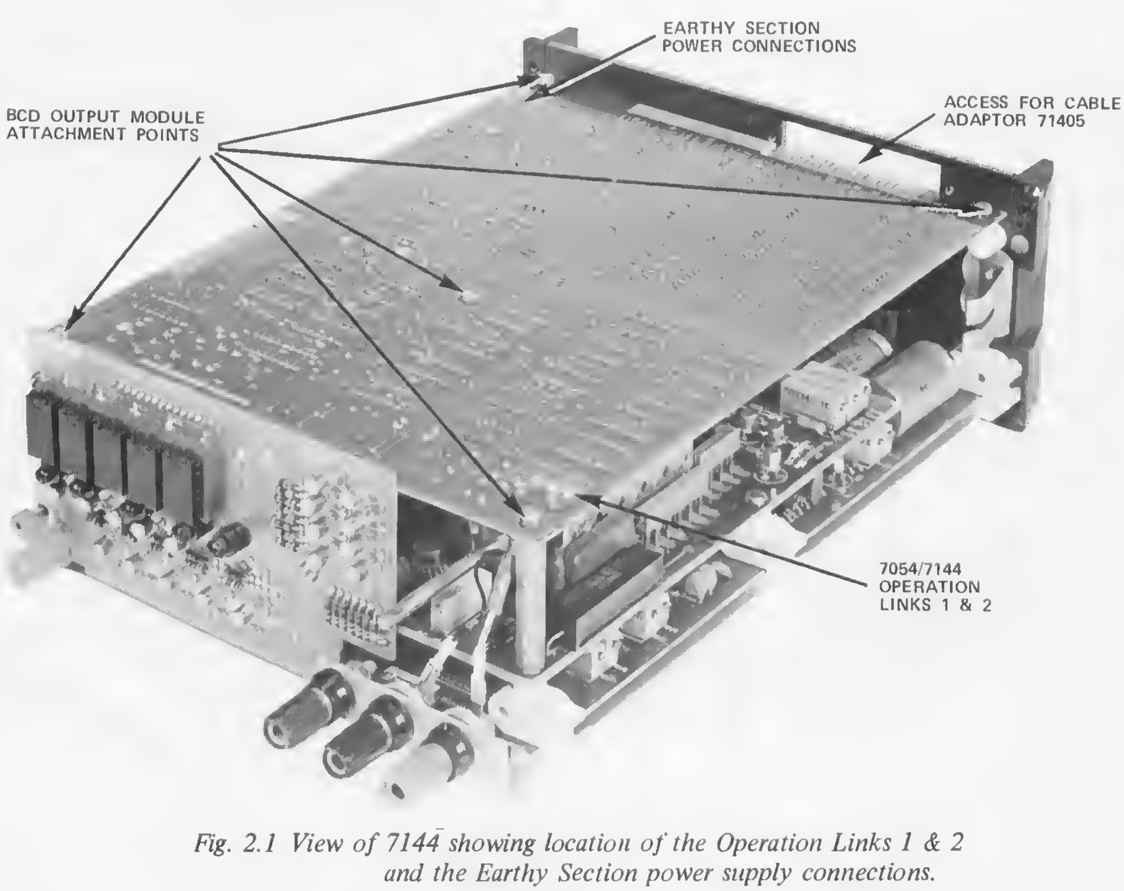


Fig. 2.1 View of 7144 showing location of the Operation Links 1 & 2 and the Earthy Section power supply connections.

(c) Refit the DMM case and connect the system using a suitable cable. This may be a cable made by the customer to suit the system being used or, if the system has been developed for use with the Solartron Master Series DVM, either of the following Cable Adaptors can be used.

70505	Cable Adaptor for the 7054 DMM
71405	Cable Adaptor for the 7144 DMM

See Diagram 13 for details of cable socket interconnections on the Cable Adaptors.

OPERATION

The operation of the BCD Output Module is dependent on the operation of the DMM (see relevant section of the manual), and on the operation of the peripheral and its interface. For those, reference to their Operating Manuals will be required.

The recording rate of the system is governed by the slowest unit and, should the peripheral interface be run at a rate exceeding the BCD Output Module capabilities, updating will cease. See Section 6 for relative pulse widths and rates.

SECTION 3 Servicing

This section provides detailed servicing information for the BCD Output Module.

INTRODUCTION

The Servicing Section is based on the functional block system of circuit diagrams, whereby components are grouped together to form a functional entity.

The BCD Output Module is divided into two main functional blocks as shown in Fig. 3.1.

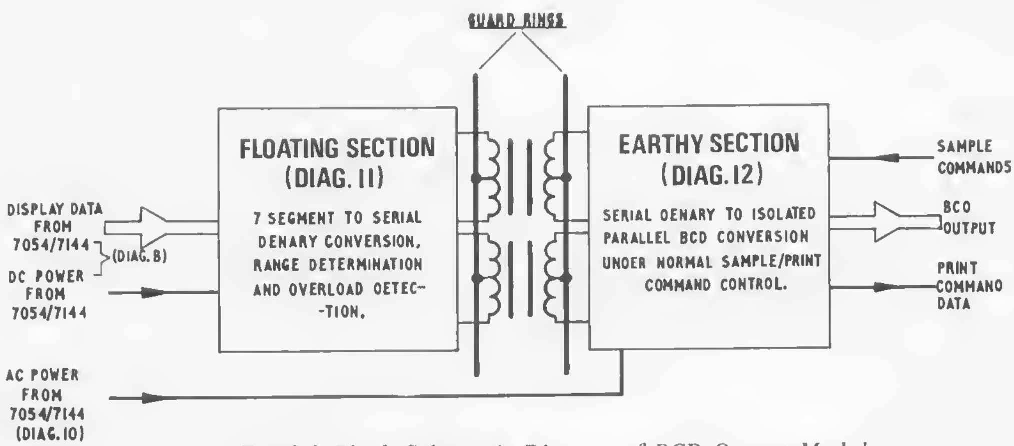


Fig. 3.1 Block Schematic Diagram of BCD Output Module.

Diagrams 11 and 12 are the two block circuit diagrams of the BCD Output Module circuit. Diagrams 1 to 10 can be found in the DMM manual.

Information regarding circuit descriptions, component locations, printed circuit board layouts, and any specific cautionary notes concerning components or testing procedures are arranged to be fully visible with the appropriate circuit diagram.

PRESENTATION OF INFORMATION

The block circuit diagrams are arranged to fold out clear to the right, with a functional description of each on the left hand text pages. The pcb layout diagram is arranged to fold out clear to the left, allowing cross reference between diagram and component location.

The functional signal flow is conventional, from left to right, with feedback lines from right to left. These rules, although generally followed, are not rigidly adhered to, due to the intricacies associated with logic circuitry. Arrows are extensively employed to indicate the direction of the logic flow.

The type of CLOCK (CK), SET (S) and RESET (R) pulses required for the less common logic devices employed are identified before each circuit description is attempted. See also Basic Logic Elements (SECTION 3).

COMPONENT LOCATION

Each circuit diagram and printed circuit board diagram are so arranged that they can be viewed together, thus aiding the identification and location of each component.

POWER RAIL NOTATION

The power rails are shown as short detatched bars with the nominal voltage annotated. All bars annotated with the same voltage are electrically connected together and correspond to the appropriate rail annotation on their respective power supplies.

The 0V rail of the 'floating section' (DIAGRAM 11) is connected to 0V on pcb 1 of the 7054/7144 DMM. The 0V (E) rail of the 'earthy section' is normally earthed at the 7054/7144 mains power supply earth but can, if required, use the peripheral earth.

It must be remembered that the voltages shown are approximate, being proportional to the load taken through the appropriate decoupling resistors. A voltage reading which is inconsistant with the value given on the diagram should not, therefore, be taken as a symptom of unserviceability without reference to other indications.

ELECTRICAL CONNECTIONS

The input to the BCD Output Module is by a 20 way Berg pin plug/socket connection and the output connector used is a 40 way BICC Burndy connector.

Transformer connections to the 'earthy section' power supply are by disconnect pins.

Connection between the floating section and the 'earthy section' is by transformer coupling, complete with guard ring protection.

Link Pins

One set of link pins render the BCD Output Module suitable for the 7054 and the 7144 DMM, identified by DMM type number.

Spare ICs

Unused ICs have their inputs connected to one of the voltage rails.

WARNING

CMOS Integrated Circuits are used on this pcb.

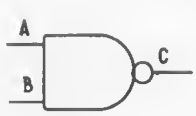
It is therefore advisable to take every precaution to reduce the risk of their damage by static charges.

BASIC LOGIC ELEMENTS

Positive logic is employed in the BCD Output Module, and the following devices are used extensively. Their logical functions are explained in the accompanying truth tables where:-

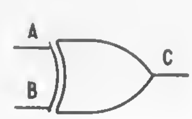
I = Hi = Bit present

0 = Lo = Bit absent



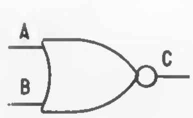
NAND Gate

A	B	C
0	0	I
I	0	I
0	I	I
I	I	0



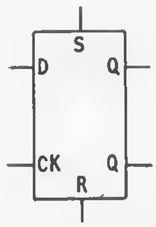
Exclusive - OR Gate

A	B	C
0	0	0
I	0	I
0	I	I
I	I	0



NOR Gate

A	B	C
0	0	I
I	0	0
0	I	0
I	I	0



D Type Flip-Flop

INPUTS				OUTPUTS		
CLOCK	DATA	SET	RESET	Q	$\bar{Q}$	
_┌¯	0	0	0	0	I	
_┌¯	I	0	0	I	0	
¯┐_	X	0	0	Q	$\bar{Q}$	*
X	X	0	I	0	I	
X	X	I	0	I	0	
X	X	I	I	INV	INV	

_┌¯ = Level Change X = I or 0

* = No Change INV = Invalid

SALIENT FEATURES OF PCB

The various important features of the 7054/7144 BCD Output Module are identified in Fig. 3.2. Plug PLC is a 40 way, double sided edge connector and, in order to ensure correct orientation with the 70505/71405 Cable Adaptor socket, a slotted keyway has been incorporated.

NOTE:- Test Edge Connectors A and B are used during production testing in the factory but may be used when fault finding.

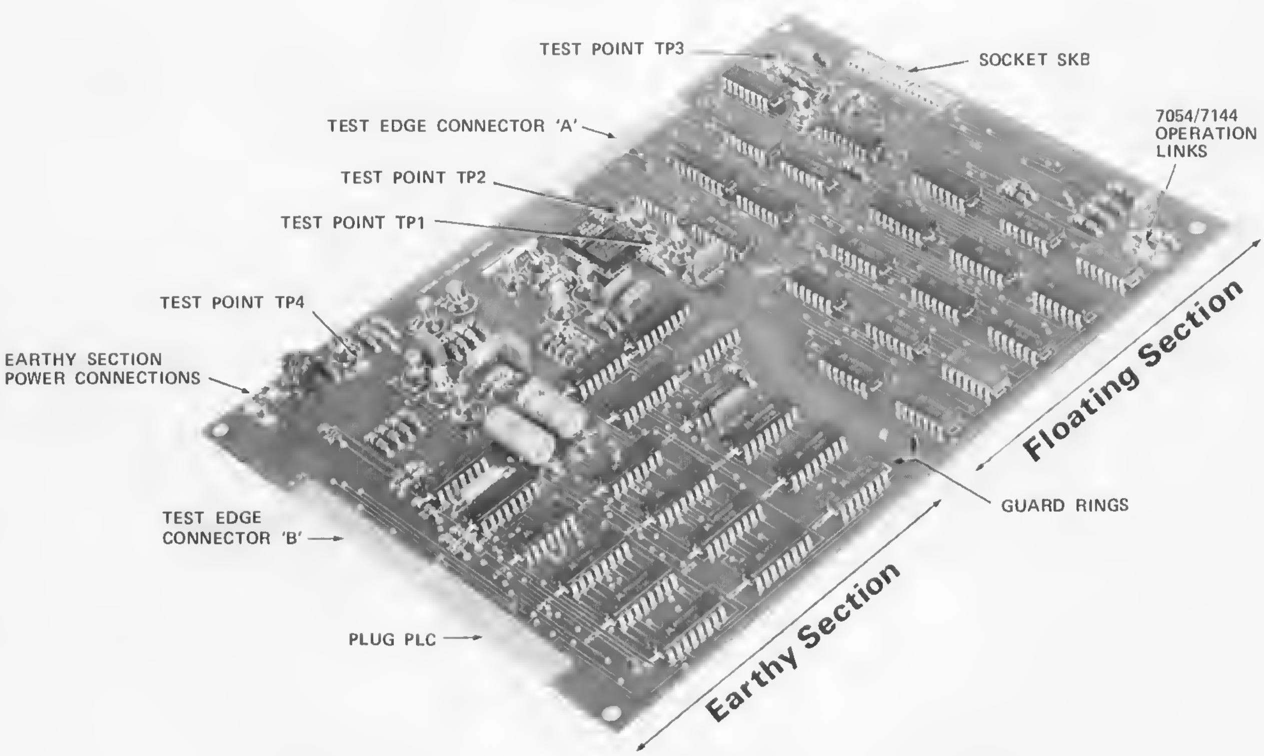


Fig. 3.2 Salient Features of the BCD Output Module.

FUNCTIONAL DESCRIPTION (FIG. 3.3)

Four parameters from the 7054/7144 DMM are used to control the operation of the BCD Output Module. They are:-

Drift Correct Pulse. Clock Pulse. First Decade Character Drive (A1). Second Decade Character Drive (A2).	$\Bigg\}$ See Diagram 8 of DMM (PLB)

The conversion of the 7 segment display data into the isolated parallel BCD output is achieved in two stages, being converted into serial denary first. For this only five of the 7 segment drives are required, with the decimal point drive line needed to determine the range.

The earliest time the BCD Output Module can use new data in any given measurement sequence is decided by the 'display load' command, internally generated in 1C7 pcb 1 of the DMM. This waveform is inaccessible, and the substitute used is the DRIFT CORRECT pulse leading edge with a 40 CLOCK pulse initiated delay added. The data conversion into serial denary commences on the arrival of the first A1 pulse after the 40 pulse count. A five state Control Counter controls this and other operations of the Module. The five states are:-

S0:- Control Counter reset

S1:- Allocation of New Data Aquisition (DRIFT CORRECT period starts)

S2:- Calculation of Acquisition Start Time (40 CLOCK pulses after S1)

S3:- New Data Conversion to serial denary (First A1 pulse after S2)

S4:- Range Determination (Second A1 pulse after S2)

S0:- Control Counter reset (Third A1 pulse after S2 followed by the end of DRIFT CORRECT pulse)

During state S3, the five segment drive lines are compared with five outputs of a decade counter driven BCD - 7 segment decoder. The decade counter is arranged to count up to 10 for every drive period, being driven by CLOCK ÷ 2 pulses. A comparator detects when parity exists between the two sets of outputs and latches the decade counter clock, thus producing a 7 segment to serial denary conversion, e.g. a 7 segment input of 3 produces three output clock pulses during that decade drive period. At the end of each decade drive period an END OF DECADE pulse is generated.

The serial denary pulses, produced during states 3 and 4, and the END OF DECADE pulses are fed to the 'earthy section' via two transformers. The END OF DECADE pulses clock an 8 bit shift register which, if a sample has been called for, selects in turn each of seven counters and steers the serial denary pulses to be counted, starting with the most significant decade, A1. The BCD counters store the BCD output information until the next sample is called for.

The seventh counter is used to store the BCD range number. This is not determined until state S4 of the Control Counter sequence. The range number is derived from the position of the decimal point, this being further modified by the instrument mode and the setting of the 7054/7144 link in the 'floating section' of the pcb.

An overload condition is identified by detecting a '1' during the A1 drive period followed by a blank A2 drive period (Decade drives A2 to A6 are blanked by the LS1 MOS integrated circuit on DMM pcb 1). The BCD output depicting an overload condition is decimals ± 110000 for the 7054 and ± 11000 for the 7144.

State S4 ends with the arrival of the third A1 pulse, this resets the Control Counter to state S0 and in doing so initiates all the other required resets. When the DRIFT CORRECT pulse ends, the positive going edge is used as a check reset of the Control Counter.

All BCD outputs are buffered to maintain TTL compatibility.

The normal sample/print command closed loop system is used as defined in the specification Section (SECTION 6).

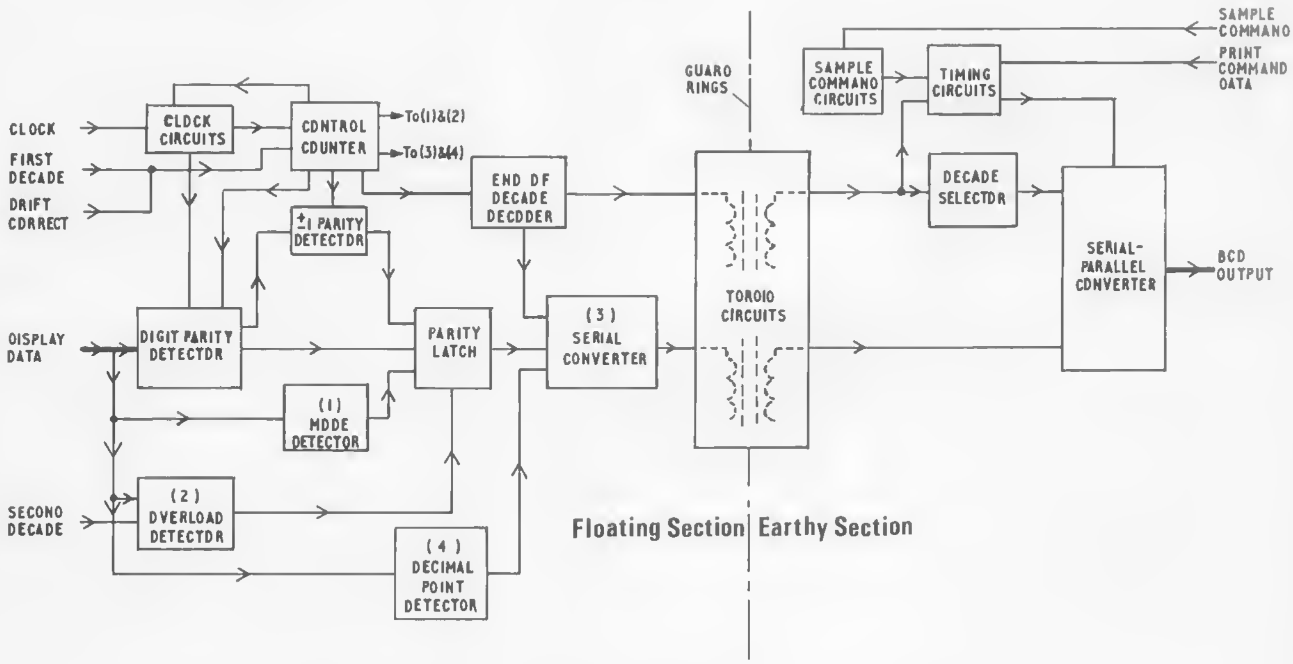


Fig. 3.3 Functional Block Schematic Diagram of BCD Output Module.

TEST WAVEFORMS

Four test points, TPs 1 to 4, are incorporated on the pcb, providing the following facilities.

TP1:- For examination of the END OF DECADE pulses.

TP2:- For examination of the DENARY pulses.

TP3:- Useful where synchronisation with the DMM Clock is required.

TP4:- Provides a monitoring point for the +5V supply voltage.

An example of a typical CLOCK waveform is shown in the DMM Technical Manual, identified under Frame 3B - 5.

The following test waveforms illustrate the output from the Serial Converter and the End of Decade Decoder during Control Counter states 3 (Decades A1 to A6 on illustration) and 4 (Range Number on illustration) on a 7054 DMM.

NOTE:- The Serial Converter pulses during Range Number determination can be entirely CLOCK ÷ 20 pulses or CLOCK ÷ 2 and CLOCK ÷ 20 pulses, dependent on the DMM measurement mode.

FRAME 3 - 1

UPPER TRACE

This is taken from TP2, oscilloscope settings

Time/cm = 200μs

Volts/cm = 5V

The serial denary pulses are clearly seen and when counted from the left, give:-

Decades	Pulses	BCD Output	Readout
A1:-	1 (CK ÷ 2)	–VE sign	–
A2:-	1 (CK ÷ 2)	001	1
A3:-	2 (CK ÷ 2)	010	2
A4:-	3 (CK ÷ 2)	011	3
A5:-	4 (CK ÷ 2)	100	4
A6:-	5 (CK ÷ 2)	101	5
Range Number:-	4 (CK ÷ 20)	100	4

Mode is '**V.DC**'

Interpretation of Module output = INTEGRATOR OUTPUT x 10^{-n}V where n = Range Number

= -12345×10^{-4}V

= -1.2345V

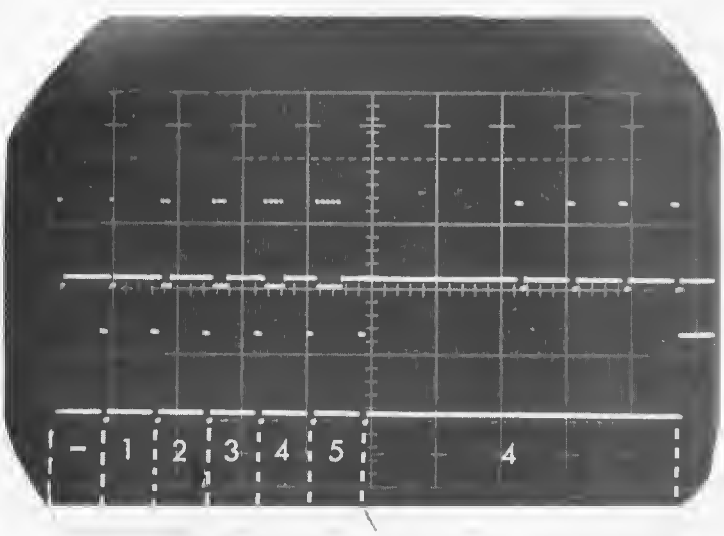
LOWER TRACE

This is taken from TP1, oscilloscope settings

Time/cm = 200μs

Volts/cm = 5V

The END OF DECADE pulses are clearly seen, including the effect on test point TP1 as the Control Counter reverts to state S0.



Decades A1 to A6 Range Number

Frame 3.1

FRAME 3 - 2

It can be seen that the serial denary pulse count during Control Counter state S3 (Decades A1 to A6 on the illustration) are identical to those of Frame 3 - 1. The Range Number, however, differs in that the Mode Detector has introduced the three extra CLOCK ÷ 2 pulses which, when added to the two CLOCK ÷ 20 pulses, give a Range Number of 5.

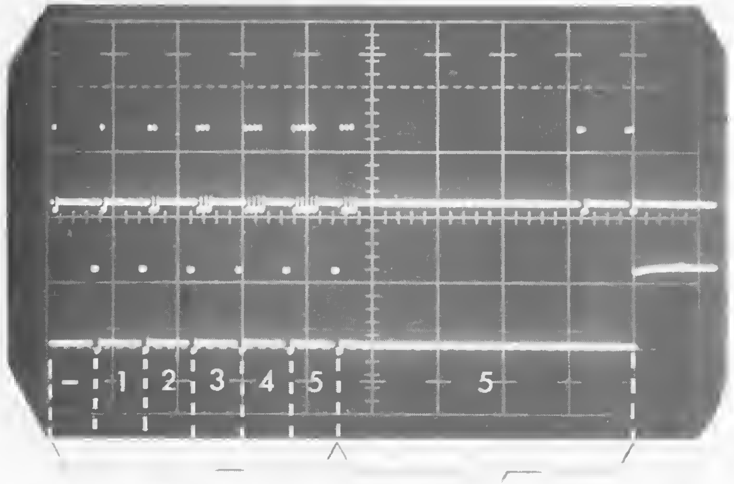
i.e. Interpretation of Module output = -12345×10^{-5} V (Mode is 'V.DC')

= $-.12345$V

= -123.45mV

The oscilloscope settings are the same as Frame 3 - 1.

The remaining frames, at the same oscilloscope settings as Frame 3 - 1, illustrate the following Module output interpretations.



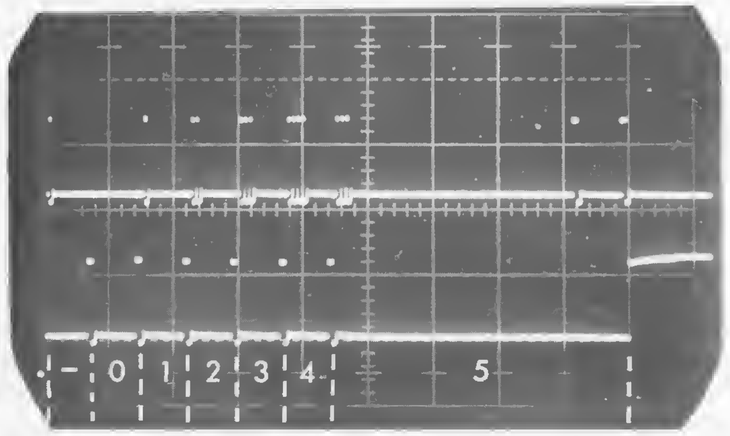
Decades A1 to A6 Range Number

Frame 3.2

FRAME 3 - 3

Interpretation of Module output = -01234×10^{-5} V (Mode is 'V.DC')

= $-.01234$V



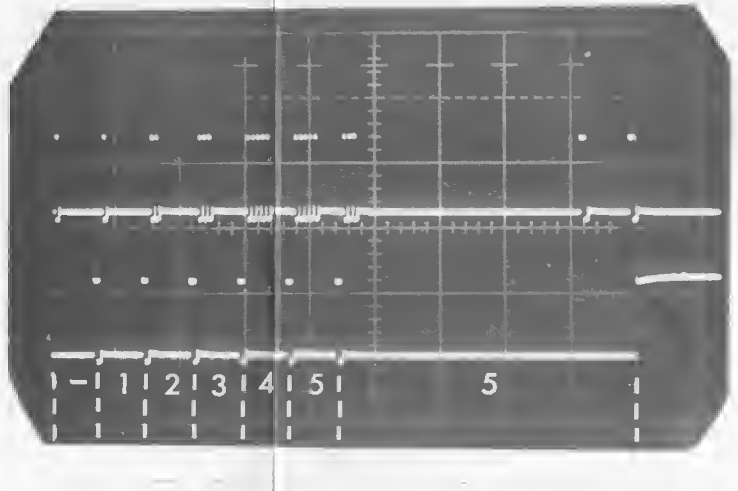
Decades A1 to A6 Range Number

Frame 3.3

FRAME 3 - 4

Interpretation of Module output = 12345×10^{-5}mA (Mode is 'μA.DC')

= $-.12345$mA



Decades A1 to A6 Range Number

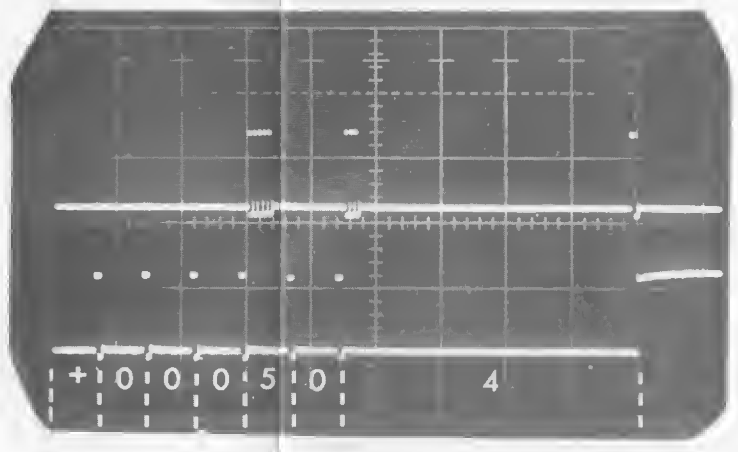
Frame 3.4

FRAME 3 - 5

Interpretation of Module output = $+00050 \times 10^{-4}$kΩ (Mode is Ω)

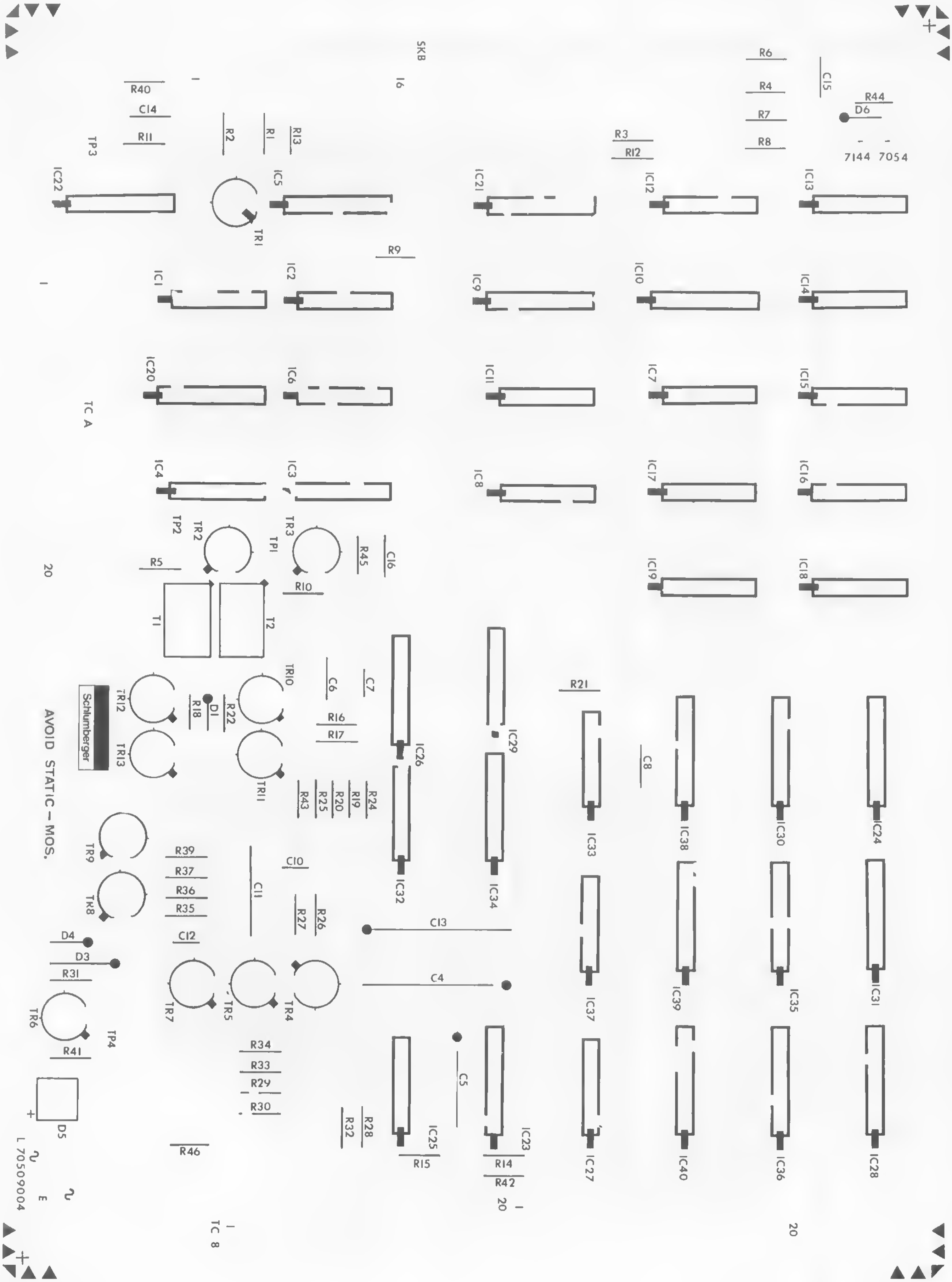
= $+0.0050$kΩ

NOTE:- Decade A1 has no pulse i.e. indicating + sign.



Decades A1 to A6 Range Number

Frame 3.5


AVOID STATIC – MOS.
Schlumberger
L 70509004
7144 7054
SKB
TC A
TC B
TP1
TP2
TP3
TP4
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
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T2
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TR6
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TR8
TR9
TR10
TR11
TR12
TR13
IC1
IC2
IC3
IC4
IC5
IC6
IC7
IC8
IC9
IC10
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IC12
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IC14
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IC16
IC17
IC18
IC19
IC20
IC21
IC22
IC23
IC24
IC25
IC26
IC27
IC28
IC29
IC30
IC31
IC32
IC33
IC34
IC35
IC36
IC37
IC38
IC39
IC40
16
20

FRAME 3 - 6

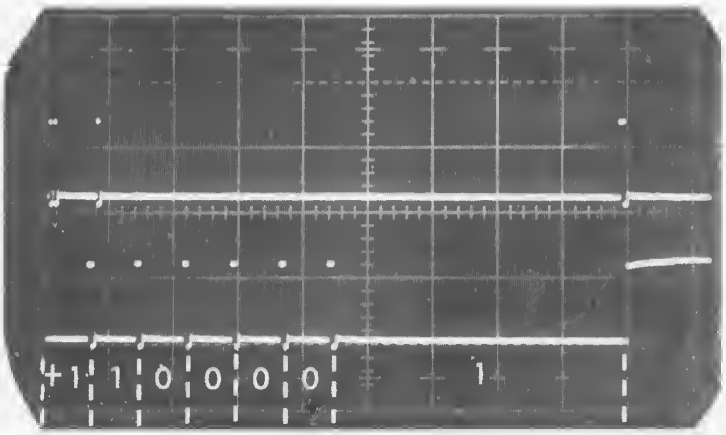
This is the OVERLOAD indication when the instrument is in the Ω mode.

OVERLOAD INDICATIONS

The following OVERLOAD indications exist for the modes and instrument type stated:-

MODE	7054	7144
V.AC/V.DC	± 110000 2	± 11000 1
Ω	+ 110000 1	+ 11000 0
μA.DC	± 110000 2	± 11000 1

the last digit being the Range Number.



Decades A1 to A6 Range Number

Frame 3.6

← *Fig. 3.4 PCB COMPONENT AND COPPER TRACK LAYOUT.*

SUB-SECTION 3a-Floating Section

This sub-section deals with the conversion of the 7 Segment Display data from the DMM into Serial Denary pulses for further transformation into BCD in the 'earthy section' (SUB-SECTION 3b).

FUNCTIONAL DESCRIPTION (DIAGRAM 11)

SEQUENCE CONTROL

The Control Counter is switched through it's various states by the DRIFT CORRECT, 1st DECADE (A1) and CLOCK ÷ 20 pulses. Whilst in it's various states, the Control Counter enables selected gates in other functional blocks, and applies the necessary SETS and RESETS throughout the circuit.

The Clock Divider produces the CLOCK ÷ 2 and CLOCK ÷ 20 pulses during all Control Counter states except S2 (the wait period between the end of the 40 pulse count and the arrival of the following A1 pulse). The CLOCK ÷ 2 pulse is used as the gating pulse for the serial denary pulses. The CLOCK ÷ 20 pulse is used to produce the END OF DECADE pulse, and is also used as the 'counting pulse' for Decimal Point detection.

CIRCUIT ACTION

It is assumed that the Control Counter sequence is in state S0.

State S0:- All circuit RESETS are applied and the CLOCK pulses are inhibited in the Clock Divider. The DRIFT CORRECT period starts and the –ve going edge of it's waveform switches the Control Counter to state S1.

State S1:- The RESETS are removed from the two decade counters and the Clock Divider is enabled, allowing CLOCK pulses to be counted. A pulse is generated by the End of Decade Decoder to initiate the serialise delay in the Timing Circuits (DIAG. 12). Both Parity Detectors operate continuously during the decade counter's counting periods but their outputs to the Parity Latch are disabled by the Control Counter, thus no pulses are allowed through the Serial Converter. After 40 CLOCK pulses have been counted through the Clock Divider, the Control Counter goes to state S2.

State S2:- The Clock Divider is disabled, producing no output pulses. The Parity Latch is still disabled. The first A1 pulse arrives, taking Control Counter to state S3.

State S3:- The following circuits are enabled for one complete cycle of display multiplexing, to allow determination of digit and overload information:-

± 1 Parity Detector
Digit Parity Detector
End of Decade Decoder
Serial Converter
Overload Detector

While decade A1 bar data are applied, CLOCK pulses are gated through the Serial Converter until parity is detected by the ± 1 Parity Detector. The Parity Latch is then operated, disabling the Serial Converter. Also during the A1 data application, the Overload Detector is searching for a possible overload condition, i.e. the presence of a '1'. At the end of decade A1, the End of Decade Decoder produces the END OF DECADE pulse and also generates the Parity Latch RESET pulse. Decade A2 bar data are then applied and CLOCK pulses gated through the Serial Converter until parity is detected by the Digit Parity Detector, when the Parity Latch will again be operated,

disabling the Serial Converter. Simultaneonsly, the Overload Detector analyses A2 and, should A2 be fully blanked, it will operate the Parity Latch using the SET input. Otherwise, the Overload Detector holds off this SET action. Again an END OF DECADE pulse is generated along with the Parity Latch RESET pulse. Decades A3 to A6 receive similar treatment from the Digit Parity Detector and Parity Latch.
When the next A1 pulsc arrives, the Control Counter goes to state S4.

State S4:- The following circuits are disabled, allowing determination of range information only:-

± I Parity Detector
Digit Parity Detector
End of Decade Decoder
Overload Detector

The RESET is removed from the Decimal Point Detector, and the Mode Detector is enabled. Decade A1 bar data are searched for the presence of either modes Ω, mV or μA. If one of those modes is present, the operation of the Parity Latch is delayed by 3 decade counter (Clock Divider) counting pulses, which are counted through. Decades A2 to A6 are then searched by the Decimal Point Detector until the decimal point is found, after which CLOCK ÷ 20 pulses (one for each decade after decimal point detection) are gated through the Serial Converter.
i.e. Pulses counted during state S4 consist of:-

For modes Ω, mV or μA:-

3 serial denary pulses and 1 CLOCK ÷ 20 pulse per decade after the decimal point detection.

All other modes:-

1 CLOCK ÷ 20 pulse per decade after decimal point detection.

NOTE:- In the case of the 7144 Module, the Decimal Point Detector is arranged to delay the gating of the CLOCK ÷ 20 pulses after decimal point detection, causing the loss of one CLOCK ÷ 20 pulse. This is to compensate for the difference in scale lengths between the 7054 and 7144.

When the next (third) A1 pulse arrives the Control Counter goes to state S0, applying all the RESETS.

State S0:- All circuits are rcset, and when the DRIFT CORRECT period ends, the +ve going cdge of it's waveform is used to carry out a 'check rcset' on the Control Counter.

The circuit descriptions of the individual functional blocks in the 'floating section' follow.

CONTROL COUNTER

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

ICs 16, 17 and 19/1-5:- (a) Produce the required logic levels at points S0 to S4 in the correct sequence, thus controlling the operation of the various functional blocks in the circuit.

(b) Control the reset of
(a) Decade counters, IC10.
(b) Decimal Point Detector, IC13 (b).
(c) Parity Latch, IC4 (a).

IC7/11-13:- Activates decade counter reset during Control Counter states S0 and S2.

C15/R44/D6 differentiate the +ve going edge when the DRIFT CORRECT period ends, providing a 'check reset' pulse.

IC13(a):-	Produces CLOCK ÷ 40 pulses at $\bar{Q}$ output.
ICs 14 (3 gates) & IC15:-	Control the switching sequence of ICs 16 and 17 as shown in Tables 3a.1 and 3a.2, with IC15/9 providing the common clock input.

IC 14 PIN NUMBERS									IC 15 PIN 9	CIRCUIT SEQUENCE
8	9	10	12	13	11	5	6	4		
0	1	1	1	0	1	0	0	1	0	State S0 assumed.
0	1	1	1	1	0	0	0	1	1	DRIFT CORRECT period starts (–ve going edge).
1	1	0	0	1	1	0	0	1	1	Counter goes to state S1. The 40 CLOCK pulse count starts.
1	0	1	0	1	1	0	0	1	0	After 20 CLOCK pulses.
1	1	0	0	1	1	0	0	1	1	40 CLOCK pulse count completed.
0	1	1	0	1	1	1	0	1	0	Counter goes to state S2, waiting on the first decade A1 pulse.
0	1	1	0	1	1	1	1	0	1	First decade A1 pulse arrived.
0	1	1	0	1	1	1	1	0	1	Counter goes to state S3, data conversion starts with A1.
0	1	1	0	1	1	1	0	1	0	Decades A2 to A6 are processed.
0	1	1	0	1	1	1	1	0	1	Second decade A1 pulse arrives.
0	1	1	0	1	1	1	1	0	1	Counter goes to state S4. Range determination starts.
0	1	1	0	1	1	1	0	1	0	Second decades A2 to A6 are scanned for decimal point.
0	1	1	0	1	1	1	1	0	1	Third decade A1 pulse arrives.
0	1	1	1	1	0	0	0	1	1	Counter reverts to state S0, resets activated.
0	1	1	1	0	1	0	0	1	0	DRIFT CORRECT pulse ends, providing 'check reset' pulse.

Table 3a.1

COUNTER STATE	OPERATING FUNCTION	IC16		IC17		IC19
		Q.1	Q.13	Q.1	Q.13	1
S0	END OF DRIFT CORRECT (VIA C15)	1	0	0	0	0
S1	START OF DRIFT CORRECT	0	1	0	0	0
S2	STATE S1 + 40 CLOCK PULSES	0	0	1	0	0
S3	FIRST A1 PULSE AFTER S2	0	0	0	1	0
S4	SECOND A1 PULSE AFTER S2	0	0	0	0	1
S0	THIRD A1 PULSE AFTER S2	1	0	0	0	0

Table 3a.2

Table 3.2 shows the states of the Q outputs of ICs 16, 17 and the output of IC19 as the sequence detailed in Table 3.1 occurs.

CLOCK DIVIDER

DECADE COUNTER LOGIC

CLOCK	INHIBIT	RESET	ACTION
⌐L	0	0	INCREMENT COUNTER
⌐L	1	0	COUNTER INHIBITED
X	X	1	ALL OUTPUTS GO TO 0

⌐L = Level Change X = 1 or 0

CIRCUIT DESCRIPTION

IC1 :- Gates the CLOCK pulses.

IC4(b) :- Produces CLOCK ÷ 2 pulses.

IC10(a) :- Performs two functions:-

(a) Produces the BCD output to feed the BCD to 7 segment decoder, IC9.

(b) Together with IC4(b) and IC14/1-3 produces a CLOCK ÷ 20 trigger pulse for IC13(a) and the End of Decade Decoder.

END OF DECADE DECODER

IC8/8-10 :- Gates the CLOCK ÷ 20 pulses during state S3 i.e. 1 pulse per decade scanned.

IC8/11-13 :- 1. Gates the END OF DECADE pulses received from IC8/10.

2. Is enabled by the arrival of DRIFT CORRECT and this action produces the trigger pulse for the serialising delay monostable, IC26(b), (DIAGRAM 12).

± 1 PARITY DETECTOR

DECADE COUNTER LOGIC

CLOCK	INHIBIT	RESET	ACTION
⌉_	0	0	INCREMENT COUNTER
⌉_	1	0	COUNTER INHIBITED
X	X	1	ALL OUTPUTS GO TO 0

⌉_ = Level Change X = 1 or 0

PARITY DETECTOR LOGIC

FIRST DECADE DISPLAY	DECADE COUNTER OUTPUT			NUMBER OF PULSES COUNTED
	A	B	C	
+VE (Blank)	0	0	0	0
–VE (BAR 'g')	1	0	0	1
+1 (BARs 'b' & 'c')	0	1	0	2
–1 (BARs 'b', 'c' & 'g')	1	1	0	3
———	0	0	1	INHIBITED

CIRCUIT DESCRIPTION

IC10(b) :- Counter is subjected to the normal decade count cycle but is self-inhibited on the 4th pulse.

IC2/10-13 :- Gate fully enabled when parity exists during the 1st Decade scan under Control Counter state S3.

IC11 & IC19:- These are the logic gates for the 1st Decade parity detection, with IC19 gating IC2/10-13, resulting in the denary pulse output as stated in the Parity Detector Logic table.

DIGIT PARITY – DETECTOR

BCD - 7 SEGMENT DECODER LOGIC

BCD INPUTS				7-SEGMENT OUTPUTS (5 of)					DECIMAL NUMBER
D	C	B	A	a	b	f	g	e	
0	0	0	0	1	1	1	0	1	0
0	0	0	1	0	1	0	0	0	1
0	0	1	0	1	1	0	0	1	2
0	0	1	1	1	1	0	1	0	3
0	1	0	0	0	1	1	1	0	4
0	1	0	1	1	0	1	1	0	5
0	1	1	0	0	0	1	1	1	6
0	1	1	1	1	1	0	0	0	7
1	0	0	0	0	1	1	1	1	8
1	0	0	1	1	1	0	1	1	9

CIRCUIT DESCRIPTION

IC9 :- Decodes each BCD output from IC10(a) but parity is only effected on Decades A2 to A6.

IC15 & IC7 :- Included logic to compensate for the different decimal six presentation i.e.

Input from DMM uses top segment 'a' while decoder, IC9, does not.

IC11 & IC12:- Detect parity between 'BAR' Inputs and decoder, IC9 output.

IC5 :- Performs the AND function on

(a) Parity detectors ICs 11 & 12
(b) $\overline{\text{CLOCK}}$ and CLOCK ÷ 2 pulses
(c) $\overline{\text{A1}}$ (i.e. Decades A2 to A6)

IC1 :- Gates the parity signal from IC5/14 during state S3 only.

PARITY LATCH

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

IC2 :- Gates:- (a) the parity signal from IC2/10 or
(b) the parity signal from IC1/4 or
(c) the Mode Detector signal

IC8 :- In conjunction with C14/R40 produces a reset pulse for IC4(a):-

1) Before Control Counter state S3 is selected
2) During state S3, on each END OF DECADE pulse.

IC4(a) :- The parity latch, activated as follows

On RESET:- $\overline{Q}$ is Hi with Serial Converter enabled. Unlatched.

On SET:- $\overline{Q}$ goes Lo stopping Serial Converter (Overload condition). Latched.

On CLOCK:- $\overline{Q}$ goes Lo stopping Serial Converter. Latched.

SERIAL CONVERTER

CIRCUIT DESCRIPTION

IC1/8-10 :- Enabled by IC6/8-10 during Control Counter states 3 and 4 only, transfers CLOCK pulses to gate IC3/3-6

IC3/3-6 :- Enabled by Parity Latch IC4(a), and CLOCK ÷ 2 pulses, transfer a CLOCK pulse during a CLOCK ÷ 2 period to IC3/10-13.

IC3/10-13 :- This gate transfers pulses to the Toroid Driver TR2 either from

(a) IC3/4-6 or
(b) the Decimal Point Detector.

DECIMAL POINT DETECTOR

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

IC8 :- Enabled by IC6, transfers the CLOCK ÷ 20 pulses to the Toroid Driver TR2, via the Serial Converter.

ICs13(b) & 6 :- Gate the CLOCK ÷ 20 pulses through IC8 as follows:-

Linked for 7054

$\overline{\text{BAR 'p'}}$:- $\overline{Q}$ is Hi (reset by Control Counter) holding IC6 gate off, disabling IC8.

BAR 'p' :- $\overline{Q}$ goes Lo, IC6 enables IC8, which gates CLOCK ÷ 20 pulses to the Serial Converter, one pulse for each remaining decade scanned.

Linked for 7144

$\overline{\text{BAR 'p'}}$:- $\overline{Q}$ is Hi, CK is Lo and IC6 disables IC8 as before.

BAR 'p' :- CK goes Hi taking IC6/2 with it. $\overline{Q}$ goes Lo but IC6 is still disabled.

$\overline{\text{BAR 'p'}}$:- The reversion to this state on the next decade to be scanned takes CK Lo and IC6 enables IC8. CLOCK ÷ 20 pulses are gated through, one pulse for each remaining decade to be scanned.

This skip action compensates for the smaller scale length (5 digits) of the 7144.

IC13b is held in RESET, being released during Control Counter state S4 only.

MODE DETECTOR

CIRCUIT DESCRIPTION

IC6:- Enables gate IC1 when $\overline{\text{BAR 'a'}}$ and/or $\overline{\text{BAR 'f'}}$ input conditions exist.

Note:- During the scan of decade A1 this is the condition for either of the following modes:- Ω, mV or μA.

IC7:- Delays the switching of IC1 by 3 decade counter IC10(a) counting pulses.

IC1:- Will enable IC2 if gating conditions for IC6 are present.

IC2:- Provides for delayed Parity Latch operation during the scan of decade A1, under Control Counter state S4, in modes Ω, mV or μA. Then, the Serial Converter is allowed to produce the extra 3 denary pulses. Otherwise, the Parity Latch is operated directly the decade A1 scan commences.

OVERLOAD DETECTOR

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3)

CIRCUIT DESCRIPTION

IC15:- Detects the presence of a '1' in the 1st Decade (A1) during Control Counter state S3 and produces a SET pulse for IC18(a).

IC18(a):- Conditions the data input (D) of IC18(b).

IC18(b):- Conditions the gate IC3 relative to whether the 2nd Decade (A2) is present or blanked.

The action of the two flip-flops (IC18) is dependent upon the conditions of A1 and A2 prevailing as follows:-

1. **A1:- Blank A2:- Present or blank**

IC15/3 is Lo, IC15 is disabled, no SET pulse available for IC18(a)
IC18(a) has been reset during Control Counter state S0
i.e. Q = Lo
IC18(b) held in reset condition during A1 scan
i.e. Q = Lo and IC3 is disabled.

At the end of A1 both flip-flops are released. During the A2 scan period, no change in IC18(b) output occurs as both flip-flops are clocked, since both data inputs are Lo, thus IC3 remains disabled.

2. **A1:- Present A2:- Present**

IC15 sets IC18(a) Q = Hi
IC18 (b) held in reset during A1 scan
i.e. Q = Lo

At the end of A1 both flip-flops are released. When A2 pulse arrives

IC18(a) is clocked Q = D = Lo = IC18(b) input D
IC18(b) is clocked (after IC18a) Q = D = Lo
IC3 remains disabled.

3. **A1:- Present A2:- Blank (Overload Conditions)**

IC15 sets IC18(a) Q = Hi
IC18(b) held in reset during 1st Decade scan
i.e. Q = Lo

At the end of A1 both flip-flops are released. Since A2 is missing, IC18(a) Q output remains Hi = IC18(b) input D. IC18(b) is clocked by the second pulse produced by decade counter IC10(a) and output Q goes Hi enabling IC3. This produces the latching SET pulse for the Parity Latch, thus disabling the Serial Converter.

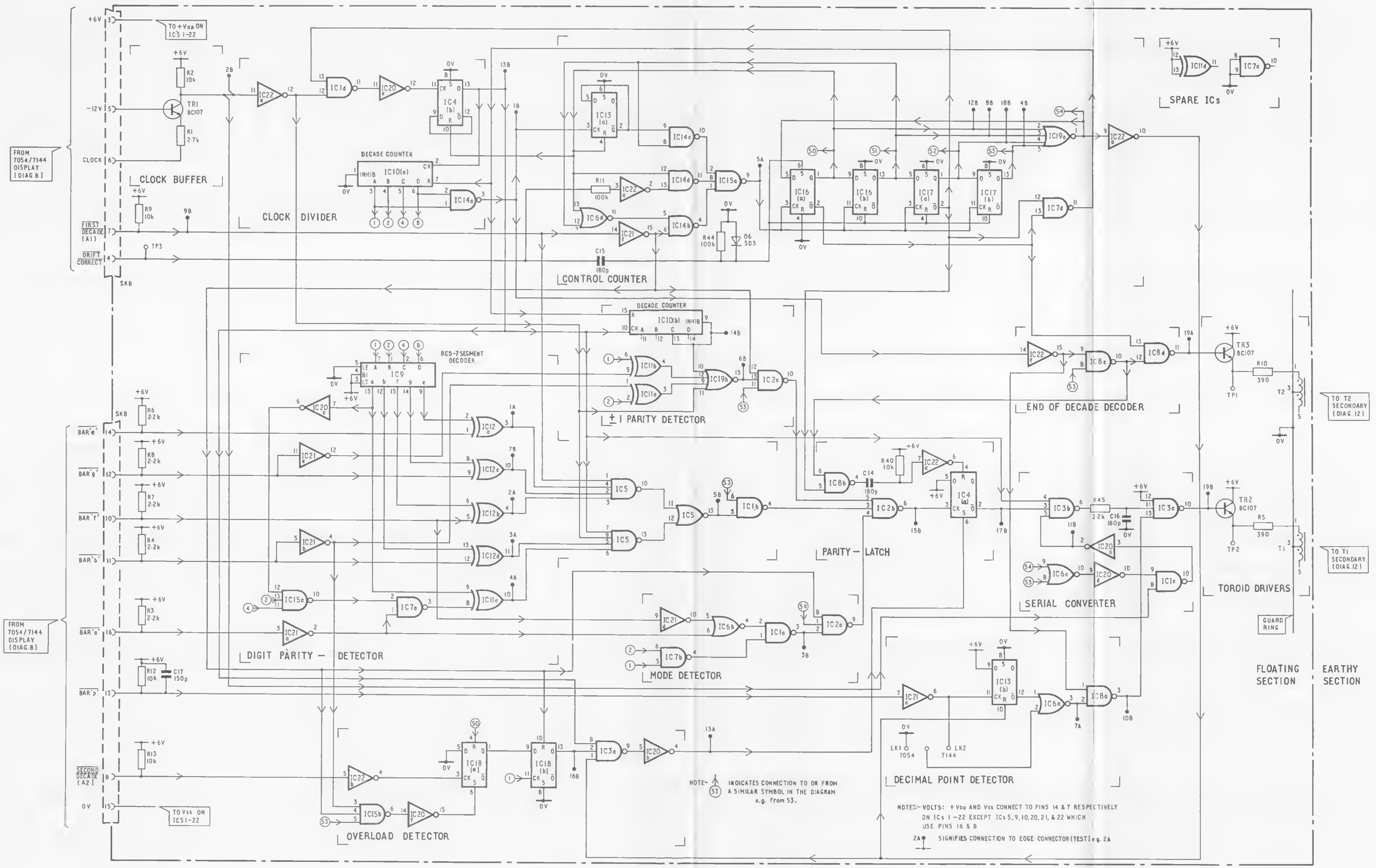
Note:- The first decade counter pulse, which would have produced decimal 0 parity, has allowed one serial denary pulse through the Serial Converter.

During A1, the ± 1 Parity Detector produces the most significant digit, +1 or – 1. The second most significant digit, 1, is produced by the single serial denary pulse allowed through the Serial Converter by delayed latching during A2.

TOROID RECEIVERS

CIRCUIT DESCRIPTION

TRs 2 and 3 receive the denary pulses and END OF DECADE pulses respectively, having as their emitter loads the primary windings of transformers T1 and T2.



See Page 3.8 for PCB LAYOUT DIAGRAMS

11 *BCD OUTPUT MODULE FLOATING SECTION CIRCUIT DIAGRAM*

SUB-SECTION 3b-Earthy Section

This sub-section deals with the conversion of the Serial Denary pulses into Isolated Parallel BCD, under the control of the normal Sample/Print Command closed loop control system.

FUNCTIONAL DESCRIPTION (DIAGRAM 12)

MODULE CONTROL

Data conversion in the earthy section is only carried out when a CONTACT SAMPLE, or a PULSE SAMPLE, has been received. Then, the Timing Circuits (Fast Rate Delay) produce a pulse which provides the DMM with a digitising period before a PRINT COMMAND is issued. The Fast Rate Delay pulse enables the gating of the serial denary pulses and counter reset pulses to the Serial-Parallel Converter. When extra time is required by the DMM, e.g. ac measurement, the DATA IS CHANGED control line can be used to switch in the Slow Rate Delay.

A Serialise Delay is incorporated, to allow sufficient time for the serial denary pulses to be steered by the Decade Selector to their respective BCD counters. The leading edge of this pulse resets the BCD counters, while its trailing edge, in conjunction with the ending of the 'sample initiated' delay, is used to produce the PRINT COMMAND pulse. As each decade is steered through, the Serialise Delay is retriggered, ensuring a full conversion before a PRINT COMMAND is given.

Two feedback signals are produced, PRINT COMMAND and DATA CAN CHANGE.

The END OF DECADE pulses are used to step the Decade Selector through the correct gate-operating sequence for the BCD counters.

CIRCUIT ACTION

The serial denary pulses from the 'floating section' are shaped by the Toroid Receiver, and fed to the Serial-Parallel Converter gate but no further, unless a sample is called for. The decade pulses shift the Decade Selector, thus enabling each BCD counter gate in turn (most significant decade first). They also re-trigger the serialise delay after each decade. These actions are continuous whilst the DMM is operating.

When a SAMPLE command is received, the Timing Circuits delays are initiated, the BCD counters are reset and the serial denary pulses are gated through to the counter by gates which are opened in sequence by the Decade Selector. The feedback signal state is:-

$\overline{\text{PRINT COMMAND LEVEL}}$

$\overline{\text{DATA CAN CHANGE}}$

The decades continue to be scanned and up-dated during the Rate Delay (sampling and digitising period). At the end of this period, and when the existing Serialise Delay pulse ends, a PRINT COMMAND pulse is generated. The feedback signal state then is:-

PRINT COMMAND LEVEL

DATA CAN CHANGE

The circuit reverts back to its non-converting state at the end of the PRINT COMMAND delay with the signal states $\overline{\text{PRINT COMMAND LEVEL}}$ and $\overline{\text{DATA CAN CHANGE}}$ again present, awaiting the next SAMPLE command.

The circuit descriptions of the individual functional blocks follow.

TIMING CIRCUITS

MONOSTABLE LOGIC (ICs 23 and 26)

1. Monostable is inhibited by the presence of a Lo on terminal 3 or 13.

2. Monostable is triggered by (a) a +ve going edge on terminal 4 or 12.
   (b) a −ve going edge on terminal 5 or 11.

   Note:- Monostable is retriggerable in both modes.

3. When triggered, terminal 6 or 10 goes Hi for time T, see Table 3b.1.

Table 3b.1

FUNCTION	TIME, T
FAST RATE DELAY (IC 23b)	0.65s $\pm$50%
SLOW RATE DELAY (IC 23a)	2.4s $\pm$25%
SERIALISE DELAY (IC 26b)	2.5ms $\pm$20%
PRINT COMMAND PULSE (IC 26a)	20μs $\pm$50%

FLIP FLOP LOGIC

See Basic Logic Elements (SECTION 3).

CIRCUIT DESCRIPTION

IC23 :- Produces the length of pulse required to match DMM operating rates when a sample is called for.

For FAST RATE:- IC23(a) is inhibited and only IC23(b) is activated by IC25/11 going Lo.

For SLOW RATE:- Both IC23(a) and IC23(b) are activated by IC25/11 going Lo.

IC26(b) :- Produces a pulse of sufficient length to allow the BCD Counters to count through two complete sets of decades.

Q going Hi:- (a) Sets IC34/7 Hi in readiness for shift register action.

(b) Produces the BCD Counter reset pulse if a sample has been called.

$\overline{Q}$ going Lo:- Sets IC29, only if a sample has been called for.

Q going Lo:- Takes IC34/7 Lo for next Decade Selection cycle.

$\overline{Q}$ going Hi:- (a) Clocks IC29 to Q = D.

(b) Removes the SET on IC29 if a sample is called for.

IC29 :- Provides the following functions:-

Q going Hi:- (a) Enables BCD counter reset gate, IC33/1.

(b) Enables data pulse gate, IC33/11.

(c) Produces DATA CAN $\overline{\text{CHANGE}}$ signal.

$\overline{Q}$ going Lo:- Produces $\overline{\text{PRINT COMMAND LEVEL}}$ signal.

Q going Lo:- (a) Disables gates IC33/1 and IC33/11.

(b) Triggers IC26(a) producing a PRINT COMMAND pulse.

(c) Produces DATA CAN CHANGE signal.

$\overline{Q}$ going Hi:- Produces PRINT COMMAND LEVEL signal.

Gates IC25 and IC37 control the set, and input D functions of IC29.

DECADE SELECTOR

SHIFT REGISTER LOGIC

Clocked operation only is used, the triggering being on the +ve going edge of the waveform, and in accordance with the following truth table.

INPUT	OUTPUTS	
DATA	Q_n	Q_n+1
0	0	0
0	1	0
1	0	1
1	1	1

$Q_n+1 = D_n$

$R = 0$

$Q_0 = A$

$Q_1 = B$ etc.

CIRCUIT DESCRIPTION

Table 3b.2 illustrates a complete serialise period and the resulting logic level changes in the shift register.

INPUTS			IC34 OUTPUTS						
FUNCTION	D1	D2	A	B	C	D	E	F	G
1. INITIAL CONDITION (Assumed)	0	1	1	1	1	1	1	1	1
2. SERIALISE DELAY INITIATED*	1	1	0	1	1	1	1	1	1
3. DECADE PULSE A1 ARRIVES	1	1	1	0	1	1	1	1	1
4. " " A2 "	1	1	1	1	0	1	1	1	1
5. " " A3 "	1	0	1	1	1	0	1	1	1
6. " " A4 "	1	1	1	1	1	1	0	1	1
7. " " A5 "	1	1	1	1	1	1	1	0	1
8. " " A6 "	1	1	1	1	1	1	1	1	0
9. RANGE DATA PULSES ARE GATED	1	1	1	1	1	1	1	1	0
10. SERIALISE DELAY ENDS (IC33 closes)	0	1	1	1	1	1	1	1	0
11. NEXT SERIALISE DELAY INITIATED*	1	1	0	1	1	1	1	1	1

* ACTIVATED BY THE DRIFT CORRECT PULSE LEADING EDGE AND RETRIGGERED BY EACH DECADE PULSE.

Table 3b.2

1. IC26(b) is in quiescence, D1 of IC34 is Lo.

2. IC32/11 goes Hi clocking IC26(b) and transferring the D1 input of IC34 to its output A. IC26(b) takes IC34 D1 input Hi.

3 - 8. The decade pulses propagate the Lo through the shift register, enabling the BCD counter gates ICs 27 and 37 in the order given in Table 3b - 2.

9. The Range data pulses are gated to the seventh BCD counter.

10. IC26(b) returns to quiescence, putting a Lo on the D1 input of IC34 in readiness for the next serialisation.

11. The next serialise delay initiating pulse clocks the Lo, retained in gate G, out of the register and starts another sequence.

SERIAL – PARALLEL CONVERTER

BCD COUNTER LOGIC

CLOCK	ENABLE.	RESET	ACTION
_/‾	1	0	INCREMENT COUNTER
X	X	1	OUTPUTS A to D go to 0

_/‾ = Level Change X = 1 or 0

FLIP-FLOP LOGIC

See Basic Logic Elements (SECTION 3).

CIRCUIT DESCRIPTION

IC33/1 :- Gates the serialise delay pulse to C8/R21 and IC33/5, producing the BCD counter reset pulse.

IC33/11 :- Gates the data pulses to IC27 and IC37.

ICs 27 & 37 :- Directs data pulses to be counted by the relevant counter ICs 24, 30, 35 and 38.

ICs 30, 35 & 38 :- Normal incrementation by the CLOCK (CK) input.

IC24 :- The counting action of these flip-flops is illustrated in Table 3b.3 with their relevant outputs. e.g. 2 pulses counted = + 100000

INPUT PULSE	IC 24(a)				IC 24(b)				OUTPUT
	CK	D	Q	$\overline{Q}$	CK	D	Q	$\overline{Q}$	
RESET	0	1	0	1	1	1	0	1	+VE(BLANK)
1st. DENARY	1	0	1	0	0	1	0	1	–VE
REST	0	0	1	0	0	1	0	1	
2nd. DENARY	1	1	0	1	1	0	1	0	100000
REST	0	1	0	1	1	0	1	0	
3rd. DENARY	1	0	1	0	0	0	1	0	–100000
REST	0	0	1	0	0	0	1	0	

Table 3b.3

ICs 28, 31, 36, 39 and 40 are the buffer stages, maintaining TTL compatibility.

Note: They use +10V and +5V power supplies.

TOROID DRIVERS

The decade and serial denary data pulses are differentiated by the transformers, T1 and T2. The transistors TRs 10 - 13 use the positive going spikes to trigger the latching circuits of IC32.

BUFFER

TRs 8 and 9 buffer IC23(a) from the driving peripheral.

DATA IS CHANGED = Hi (used to provide the extended sample and digitisation period).

SAMPLE COMMAND BUFFERS

TRs 4, 5 and 7 buffer IC25/11 - 13 from the peripheral driving circuits.

Contact Sample:- Pin 11B going Lo clocks IC23(a) and/or IC23(b).

Pulse Sample:- Pin 12B going Hi clocks IC23(a) and/or IC23(b).

IC25/11 - 13:- Produces the triggering pulses for IC23.

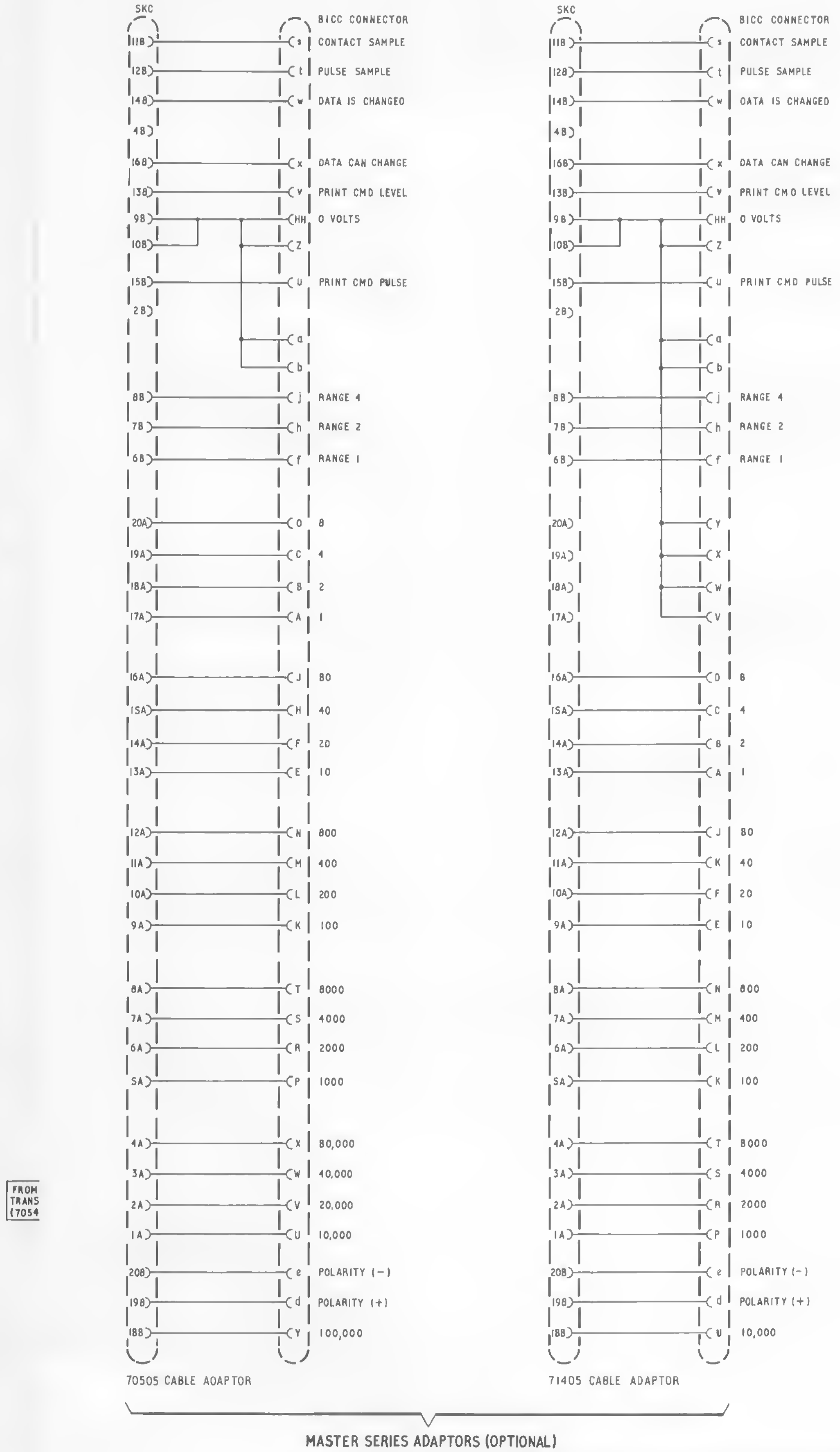
Capacitors C11 and C12 prevent triggering of the circuit by low energy noise spikes.

POWER SUPPLY

TR6, D3 and D4 provide the necessary stabilised +5V supplies for the output buffers, ICs 28, 31, 36, 39 and 40.

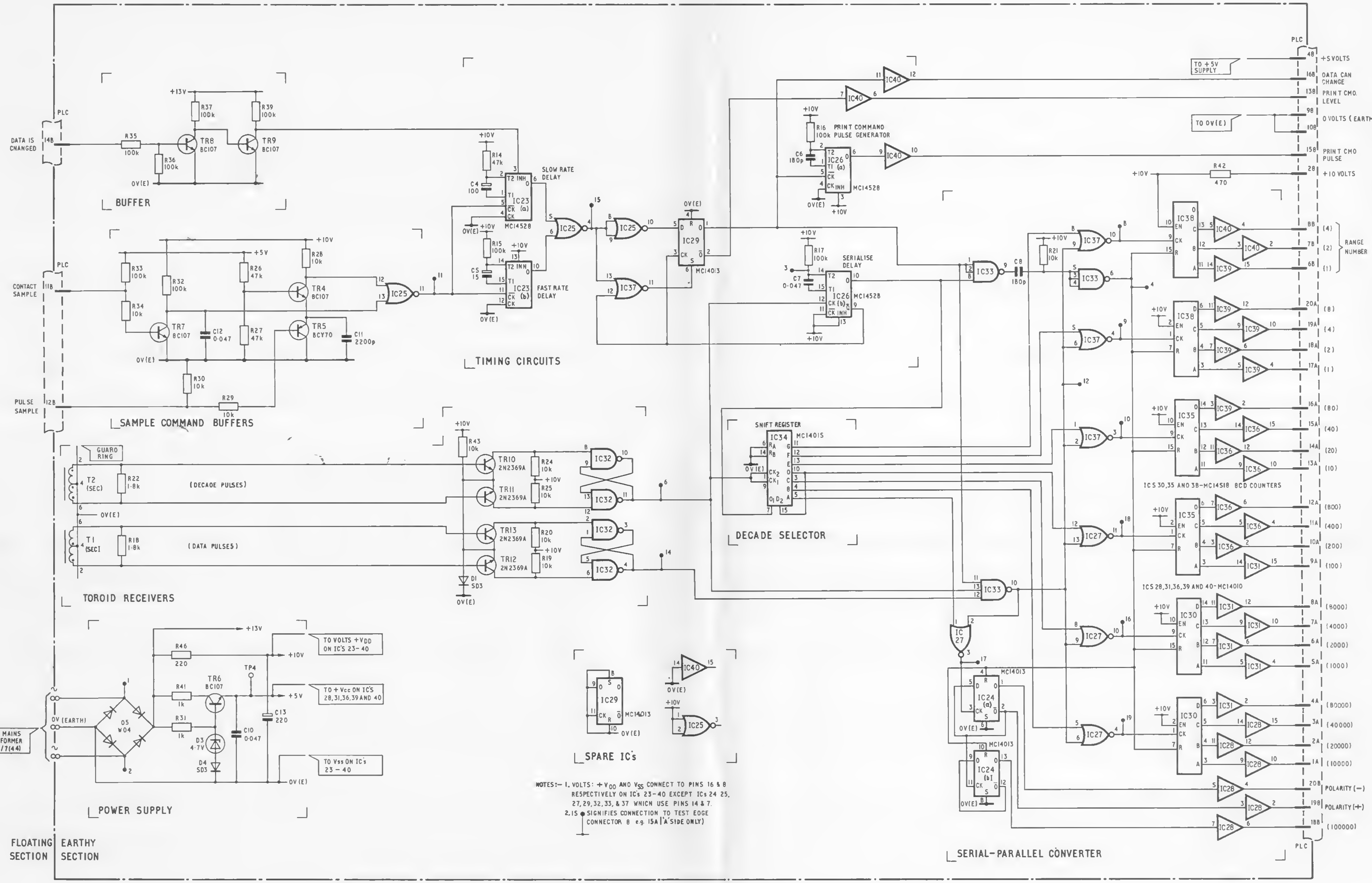
CABLE ADAPTORS 70505 AND 71405

These cable adaptors are outwardly identical, differing in the socket interconnections, as shown in DIAGRAM 13.



13 *DMM CABLE ADAPTOR CONNECTION DIAGRAMS*

◄ *DIAGRAM 12 - BCD OUTPUT MODULE EARTHY SECTION CIRCUIT DIAGRAM*



See Page 3.8 for PCB LAYOUT DIAGRAMS

12 *BCD OUTPUT MODULE EARTHY SECTION CIRCUIT DIAGRAM*

SECTION 4-Functional Checks

The tests detailed in this section check that the BCD output from the Module correlates with the value displayed on the DMM. Module testing is carried out using special test equipment, Solartron TG1308/G Output Reader. This item of test equipment is not available for purchase but details of the circuit diagram, and component parts, are shown in Fig. 4.1.

PRE - CHECK TESTS

It is assumed that the DMM is fully serviceable and that the BCD Output Module has been checked in accordance with Section 2.

The following test can now be carried out.

OUTPUT BUFFER AMPLIFIER POWER SUPPLY

1. Locate test point TP4 (near rectifier bridge D5) and the 0V (E) terminal.

2. Check that the voltage between TP4 and 0V (E) is:-

$$+4.7 \pm 0.5 \text{ Volts.}$$

PROCEDURE USING THE TG1308/G OUTPUT READER

1. Connect the TG1308/G to the DMM.

2. Switch ON the DMM and the Output Reader. Select 'VDC' on the DMM and the appropriate 7054/7144 mode on the reader.

3. Short circuit the Hi and Lo terminals of the DMM and check that the DMM reads approximately 0.00mV.

4. Set the TG1308/G to MANUAL SAMPLE, and DATA IS CHANGED to '0' (=Lo).

5. Press the MANUAL SAMPLE button and check that the Output Reader displays approximately (digit for digit correlation):-

   0.00000

NOTE:- 0.01mV is displayed on the reader as:-

0.00001

6. Set the TG1308/G to AUTO SAMPLE.

For the following inputs check that the relative readings are displayed on the DMM and the Output Reader.

NOTE:- A zero (0) and/or a positive (+) sign may be displayed in the most significant digit of the reader, dependent on type of Output Reader used.

‘VDC’ MODE

7054		7144	
D M M DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)	D M M DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)
9.00mV	+ .00900	9.00mV	+ 0900
90.00mV	+ .09000	90.00mV	+ 9000
900.00mV	+ .90000	900.0mV	+ 9000
9.0000V	+ 9.0000	9.000V	+ 9.000
90.000V	+ 90.000	90.00V	+ 90.00
900.00V	+ 900.00	900.0V	+ 900.0
– 900.00mV	.90000	– 900.0mV	– .9000
– 1.0000V	–1.00000	1.000V	– 1.0000

Ω MODE

7054		7144	
D M M DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)	D M M DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)
0.0Ω	+ 0.0000	0.0Ω	+ 0.000
900.0Ω	+ 0.9000	900.0Ω	+ .9000
9.0000kΩ	+ 9.0000	9.000kΩ	+ 9.000
90.000kΩ	+ 90.000	90.00kΩ	+ 90.00
900.00kΩ	+ 900.00	900.00kΩ	+ 900.0
9000.0kΩ	+ 9000.0	9000kΩ	+ 9000
1– – – –kΩ	+ 11000.0	1– – – –kΩ	+ 11000

‘μA’ MODE

7054		7144	
D M M DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)	D M M DISPLAY (NOMINAL)	READER DISPLAY (NOMINAL)
0.000μA	± 00000	0.000μA	± 0000
90.000μA	+ 90000	90.00μA	+ 9000
900.00μA	+.90000	900.0μA	+.9000

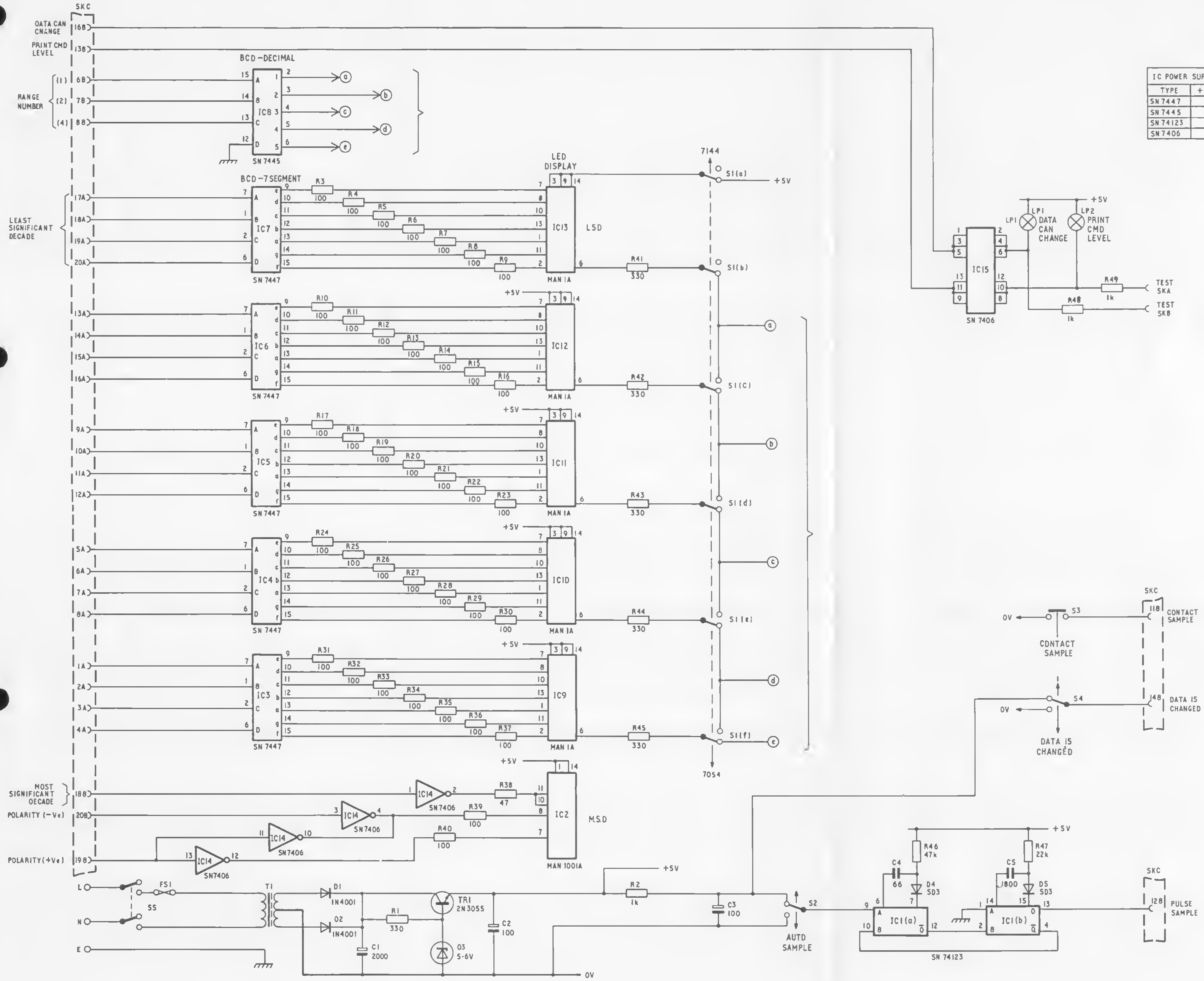
7. Set the TG1308/G to MANUAL SAMPLE.

8. Press MANUAL SAMPLE button and check:-

   After 0.9 ± 0.4 seconds (a) PRINT COMMAND LEVEL lamp lights.
   (b) DATA CAN CHANGE lamp extinguishes.

9. Set the DATA IS CHANGED to '1' (= Hi). Press the MANUAL SAMPLE button and check:-

   After 2.5 ± .5 seconds (a) PRINT COMMAND LEVEL lamp lights.
   (b) DATA CAN CHANGE lamp extinguishes.



IC POWER SUPPLY CONNECTORS		
TYPE	+5V PIN	0V PIN
SN 7447	16	8
SN 7445	16	8
SN 74123	16	8
SN 7406	14	7

Components List for Test Circuit, Fig. 4.1

Cct. Ref.	General Description		
R1	330	1/4W	10%
R2	1k	1/4W	10%
R3 to R37	100	1/4W	10%
R38	47	1/4W	10%
R39	100	1/4W	10%
R40	100	1/4W	10%
R41 to R45	330	1/4W	10%
R46	47k	1/4W	10%
R47	22k	1/4W	10%
R48	1k	1/4W	10%
R49	1k	1/4W	10%
C1	2000	30V	10%
C2	100	25V	10%
C3	100	25V	10%
C4	66	40V	10%
C5	1800p	30V	10%
D1	IN4001		
D2	IN4001		
D3	Zener 5.6V		
D4	IN914		
D5	IN914		
TR1	2N3055		
IC1	Retriggerable Monostable Multivibrator SN74123		
IC2	Light Emitting Diodes MAN 1001A		
IC3 to IC7	BCD to 7 Segment Decoder SN7447		
IC8	BCD to Decimal Decoder SN7445		
IC9 to IC13	Light Emitting Diodes MAN 1A		
IC14	Hex Inverters and Buffers SN7406		
IC15	Hex Inverters and Buffers SN7406		
LP1	Lamps 6V		
LP2	Lamps 6V		
S1	Rotary Switch (6 pole x 2 way)		
S2	Switch (1 pole x 2 way)		
S3	Button Switch (Push to make)		
S4	Switch (1 pole x 2 way)		
S5	Main ON/OFF Switch (2 pole x 2 way)		
T1	Transfer 12 - 0 - 12, 700mA		
FS1	Fuse 650mA		

NOTE:- Resistor values are in OHMS.
Capacitor values are in MICROFARADS, except when followed by a ' p ', signifying PICOFARADS.

Fig. 4.1 TG1308/G BASIC CIRCUIT DIAGRAM

SECTION 5-Parts List

Component Parts List

for

BCD Output Module 70509004

Cct. Ref.	General Description				Solartron Part No.
R1	CACP	2.7k	1/8W	±10	172032700
R2	CACP	1.0k	1/8W	±10	172041000
R3 AND R4	CACP	2.2k	1/8W	±10	172032200
R5	CACP	390	1/8W	±10	172023900
R6 to R8	CACP	2.2k	1/8W	±10	172032200
R9	CACP	10k	1/8W	±10	172041000
R10	CACP	390	1/8W	±10	172023900
R11	CACP	100k	1/8W	±10	172051000
R12	CACP	10k	1/8W	±10	172041000
R13	CACP	10k	1/8W	±10	172041000
R14	CACP	47k	1/8W	±10	172044700
R15 to R17	CACP	100k	1/8W	±10	172051000
R18	CACP	1.8k	1/8W	±10	172031800
R19 to R21	CACP	10k	1/8W	±10	172041000
R22	CACP	1.8k	1/8W	±10	172031800
R24	CACP	10k	1/8W	±10	172041000
R25	CACP	10k	1/8W	±10	172041000
R26	CACP	47k	1/8W	±10	172044700
R27	CACP	47k	1/8W	±10	172044700
R28 to R30	CACP	10k	1/8W	±10	172041000
R31	CACP	1k	1/8W	±10	172031000
R32	CACP	100k	1/8W	±10	172051000
R33	CACP	100k	1/8W	±10	172051000
R34	CACP	10k	1/8W	±10	172041000
R35 to R37	CACP	100k	1/8W	±10	172051000
R39	CACP	100k	1/8W	±10	172051000
R40	CACP	10k	1/8W	±10	172041000
R41	CACP	1k	1/8W	±10	172031000
R42	CACP	470	1/8W	±10	172024700
R43	CACP	10k	1/8W	±10	172041000
R44	CACP	100k	1/8W	±10	172051000
R45	CACP	2.2K	1/8W	±10	172032200
R46	CACP	220	1/8W	±10	172022200
C4	TANW	100	20V	±20	265881000
C5	TANW	15	20V	±20	265871500
C6	MICA	180p	500V	±5	250321800
C7	ESTM	0.047	100V	±10	225444700
C8	MICA	180p	500V	±5	250321800
C10	ESTM	0.047	100V	±10	225444700
C11	ESTF	2200p	160V	±10	221332200
C12	ESTM	0.047	100V	±10	225444700
C13	ALME	220	16V	+100 −10	273382200
C14	MICA	180p	500V	±5	250321800
C15	MICA	180p	500V	±5	250321800
C16		180p	500V	±5	250321800
C17	CERM	150p	500	±20%	241321500

Cct. Ref.	General Description				Solartron Part No.
D1	SD3				300522160
D3	Zener	4.7V	0.4W	±5	300521470
D4	SD3				300522160
D5	WO4	1A	400V		300524700
D6	SD3				300522160
TR1 to TR4	BC107				300553320
TR5	BCY70				300553590
TR6 to TR9	BC107				300553320
TR10 to TR13	2N2369				300552390
IC1	MC14011				510001660
IC2	MC14023				510001670
IC3	MC14023				510001670
IC4	MC14013				510001740
IC5	MC14501				510001710
IC6	MC14001				510001630
IC7	MC14011				510001660
IC8	MC14011				510001660
IC9	MC14511				510001850
IC10	MC14518				510001840
IC11	MC14507				510001700
IC12	MC14507				510001700
IC13	MC14013				510001740
IC14	MC14011				510001660
IC15	MC14023				510001670
IC16	MC14013				510001740
IC17	MC14013				510001740
IC18	MC14013				510001740
IC19	MC14002				510001650
1C20 to 1C22	MC 14049/CD 4049 AE				510001730
IC23	MC14528				510001770
IC24	MC14013				510001740
IC25	MC14001				510001630
IC26	MC14528				510001770
IC27	MC14001				510001630
IC28	MC14010				510001720
IC29	MC14013				510001740
IC30	MC14518				510001840
IC31	MC14010				510001720
IC32	MC14011				510001660
IC33	MC14023				510001670
IC34	MC14015				510001890
IC35	MC14518				510001840
IC36	MC14010				510001720
IC37	MC14001				510001630
IC38	MC14518				510001840
IC39	MC14010				510001720
IC40	MC14010				510001720
T1	Pulse Transformer				309605702
T2	Pulse Transformer				309605702

Component Parts List

for

Accessories - 70505/71405 Cable Adaptors

Cct. Ref.	General Description	Solartron Part No.
SKC	Connector 20 + 20 way	352520020
	Cover	33010015
	LID Moulding	33010023
	Screw M3 x 6 LG C'SK.HD. (2 off)	406403060
	Connector, 50 way Shell with Clamp	354003370
	Sockets, hyfen (36 off)	354003270
	Wire, 7/.20 x 0.3mm Wall White	
	PVC DEF 16.12	480011090

SECTION 6-Specifications

This section contains a copy of the technical specification applicable to the 7054/7144 BCD Output Module. The module is designed and manufactured to a higher specification than is claimed commercially. In order that the user may benefit as appropriate, this technical manual may relate to a superior performance. In the event of contraditions between specifications, no additional claims are made for the module above those claimed in the current product data sheet.

General

BCD Output

Type of Logic:	Positive
Scale Length:	109999 max. for 7054 10999 max. for 7144
Polarity Indications:	Positive and negative

Overload Indication:

Mode	7054	7144
V.AC	+1100.00	+1100.0
V.DC	± 11000.0	± 11000
Ω	+1100.00	+1100.0
μA*	± 1100.00	± 1100.0

*Position of decimal point is invalid.

Range Data:

Instrument Range	Range No. 7054	Range No. 7144
> 1000V	2	1
1000V	2	1
100V	3	2
10V	4	3
1V	5	4
100mV	N/A	5
> 10MΩ	1	0
10MΩ	1	0
1MΩ	2	1
100kΩ	3	2
10kΩ	4	3
1kΩ	N/A	4
> 1mA	2	1
1mA	5	4
100μA	6	5
10μA	N/A	6

N/A = Not Applicable

Environment

Working Temperature Range:	$0^{o}C$ to $+45^{o}C$
Storage Temperature Range:	$-30^{o}C$ to $+70^{o}C$
Maximum Relative Humidity:	70% at $40^{o}C$

Power Supply

Floating Section:	+ 6V (from the DMM Power Rail)
Earthy Section:	$+10V^{+3V}_{-2V}$
	+ 4.7V ± 0.5V

Output Levels

All outputs are TTL compatible and are staticised.

$+2.4V <$ logic $1 < +6.0V$

$-0.5V <$ logic $0 < +0.5V$ capable of sinking 5 standard TTL loads.

Input Levels

All inputs are TTL compatible.

Sample Command (Input)

Contact Sample: A sample is initiated by a contact closure between pin 11B and 0V for > 4ms. A current of approximately 50μA will pass through the contacts.

Pulse Sample: A positive going pulse of > 10μs duration and between 3V and 8V amplitude will initiate a sample. This pulse is applied to pin 12B on which the input impedance is approximately 10kΩ.

Data is Changed (Input)

For normal use pin 14B should be held at $+2V < V < +10V$. This is achieved by connecting pin 14B to pin 4B. In this mode of operation each measurement will take approximately 3 seconds, which allows the DMM time to change range and settle on new reading.

When it is known that the input will not change sufficiently to result in a DMM range change, the measuring time may be reduced to approximately 1 second. To do this, ensure that pin 14B is kept at $-0.5V < V < 1V$ (i.e. connect it to 0V, pin 10B).

Long period = 2.4s ± 50%

Short period = 650ms ± 50%

Numerical Output

Parallel BCD 1 - 2 - 4 - 8 code on:-

7054 DMM: Pins 1A to 20A (5 decades) with the most significant digit (100 000) on pin 18B.

7144 DMM: Pins 1A to 16A (4 decades) with the most significant digit (10000) on pin 18B.

Range Information (Output)

Data output indicating position of the decimal point is given in BCD code on pins 6B, 7B and 8B. If

n = Decimal equivalent of the BCD number

the readings conform with the equation.

Value = Reading (as an integer) x 10^{-n} V

or = Reading (as an integer) x 10^{-n} kΩ

or = Reading (as an integer) x 10^{-n} mA

Note:- The equation is incorrect for an OVERLOAD condition in the μA mode.

Polarity Output

Logical 1 on pin 19B for positive polarity.

Logical 1 on pin 20B for negative polarity.

Print Command Pulse (Output)

Positive going pulse of 10μs to 30μs duration issued on completion of a reading. May be used to stimulate a printer or similar output device.

Print Command Level (Output)

Pin 13B is held at logic 0 following a sample command and changes to logic 1 when the new reading is available at the output connector.

Data can Change (Output)

This is the complement of Print Command Level and is available on pin 16B.

Isolation

Resistance between BCD output pin 9B (0V) and the DMM front panel Lo terminal $> 10^9\Omega$ at 500V.

70505/71405 Cable Adaptor Options

Each option consists of a socket which fits into the rear of the DMM. This socket mates with the Module pcb edge connector and has it's cable terminating in a BICC BURNDY socket, so enabling direct compatibility with other Solartron equipment. The socket allocations for each option are shown in Diagram 13.